In the Claims:

1. (currently amended) A method for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process, the method comprising:

providing a processor including a plurality of analysis machines and a plurality of computer resources, wherein each of said plurality of analysis machines includes an internal pipeline and is communicably coupled to a plurality of shared pipelines, wherein each said internal pipeline is an integer pipeline that starts the execution of every instruction that executes in said analysis machine in which it is included, wherein each said analysis machine includes pre-classification hardware, wherein said pre-classification hardware classifies a plurality of packet types while data is transferred by an instruction thread of said analysis machine into a packet header memory of said analysis machine for subsequent microcode access;

executing each instruction thread in one of the plurality of analysis machines; and

sharing services of at least one of the plurality of computer resources between at least two of the plurality of analysis machines during the execution of each instruction thread.

2. (original) The method for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 1, further comprising:

transferring data from an input buffer to a packet task manager;

dispatching the data from the packet task manager to one of the plurality of analysis machines;

classifying the data in the one analysis machine;

modifying and forwarding the data in a packet manipulator.

3. (original) The method for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 2, further comprising:

transferring the data after modifying and forwarding to an output buffer.

4. (original) The method for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 1, further comprising: processing data at a rate of at least 10 Gbs.

5. (currently amended) An apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process, said apparatus comprising:

a plurality of analysis machines to execute a plurality of instruction threads, wherein each of said plurality of analysis machines includes an internal pipeline and is communicably coupled to a plurality of shared pipelines, wherein each said internal pipeline is an integer pipeline that starts the execution of every instruction that executes in said analysis machine in which it is included, wherein each said analysis machine includes pre-classification hardware, wherein said pre-classification hardware classifies a plurality of packet types while data is transferred by an instruction thread of said analysis machine into a packet header memory of said analysis machine for subsequent microcode access;

a plurality of computer resources operationally connected to said plurality of analysis machines;

wherein each instruction thread executes in one of said plurality of analysis machines, and services of at least one of said plurality of computer resources are shared between at least two of said plurality of analysis machines during the execution of each instruction thread.

6. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 5, further comprising;

a packet task manager operationally connected to said analysis machines; and, a packet manipulator operationally connected to said analysis machines.

7. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 5, wherein said analysis machines are multi-threaded.

8. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 5, wherein said analysis machines each have 32 threads.

9. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 5, further comprising:

a packet task manager operationally connected to said analysis machines; and

a packet manipulator operationally connected to said analysis machines; and

a global access bus including a master request bus and a slave request bus separated from each other and pipelined.

10. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 5, further comprising:

an external memory engine operationally connected to said analysis machines; and a hash engine operationally connected to said analysis machines.

11. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 9, further comprising:

packet input global access bus software code used for flow of data packet information from a flexible input data buffer to an analysis machine.

12. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 9, farther comprising:

packet data global access bus software code used for flow of packet data between a flexible data input bus and a packet manipulator.

13. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 9, further comprising:

statistics data global access bus software code used for connection of an analysis machine to a packet manipulator.

14. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 9, further comprising:
private data global access bus software code used for connection of an analysis machine to an internal memory engine submodule.

15. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 9, further comprising:
lookup global access bus software code used for connection of an analysis machine to an internal memory engine submodule.

16. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 9, further comprising:

results global access bus software code used for providing flexible access to an external memory.

17. (cancelled)

18. (original) The apparatus for sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process according to claim 9, further comprising:

a bi-directional access port operationally connected to said analysis machine;

a flexible data input buffer operationally connected to said analysis machine; and a flexible data output buffer operationally connected to said analysis machine.